Additional Notes

Poor Pressure Distribution

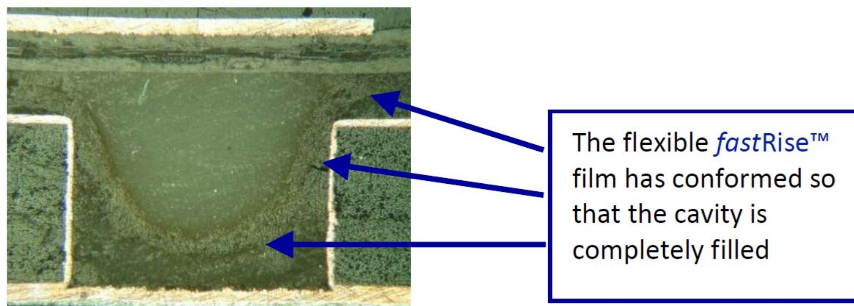
Constructions containing very low pressure areas with stacked regions of little or no copper between layers (e.g. coupons, ground clearances, fiducials, etc.) may require special considerations to achieve ideal bonding. Resin from the higher flowing fastRise™ part numbers combined with higher pressures will fill the low pressure areas to balance the pressure. Although the low flow fastRise™ may be capable, caution is advised to ensure that adequate resin flow and resin volume are present to avoid poor adhesion and resin starvation. Copper distribution should be as balanced as possible especially with thicker or plated circuits.

Multiple Ply Constructions

Resin flow can increase dramatically if multiple plies of fastRise™ are used against each other. If high-flow is not desired, pressure should be reduced by approximately 25%-50% to prevent excess resin flow, resin separation, or formation of flow channels.

Encapsulating the conductor pattern

Although fastRise™ film is not porous, it is flexible and will conform to circuit patterns. The film can have an elongation of 30-300% and will fill circuit patterns as long as there is sufficient resin to flow within the areas.



Drilling

Quick Start

The following chart is provided as a general conservative starting point for drill process development. The later sections provide substantially more detail allowing the process to be optimized for differing applications.

Please contact Technical Service for a Drill Table Creator file to calculate specific process parameters.

	Imperial units	SI units
Entry Material	Aluminum and Phenolic (0.024” preferred)	Aluminum and Phenolic (0.60mm preferred)
Backer Material	Rigid Phenolic, Slickback, or comparable	
Cutting Speed (Surface Speed)	100 SFM	30.5 MPM
Chip Load	0.0010 in	25.4 µm
Dwell	0-1000 ms (increase dwell time as speed and chip load deviate from above recommendations)	
Hit Count	25-100	

Drill Bits

Standard 130°-point geometry, 32° - 45° helix angle PCB carbide drills are sufficient to drill RF-35TC and RF-60TC laminates. Due to the highly abrasive nature of the ceramic mix used to achieve high thermal conductivity, it may be economical to consider the use of diamond-coated carbide drills for critical vias drilled in these materials. Contact your AGC technical service representative for further guidance. Stack height should not exceed 2/3 the flute length of the smallest diameter drill being used.

Sharp drill bits are critical to any PTFE drilling; new drill bits should always be used. Undercut drill bits are recommended, but past studies have shown that some drill bit brands may obtain better results using their standard drill bits.

Chip Load

A nominal chip load of 0.001" (25 µm) is a recommended starting point for all tool sizes. Some fabricators have found success in the range of up to 0.002" (50 µm). This will vary depending on types of The following chart is provided as a general conservative starting point for drill process development. The later sections provide substantially more detail allowing the process to be optimized for differing applications.
Please contact Technical Service for a Drill Table Creator file to calculate specific process parameters.
machines and drill bits being used and should be tested or proven out at each facility. Non-critical vias (RF ground stitching or heat dissipation vias) will obviously have wider processing windows. Higher chip loads generally produce more heat on the drill bit, which will lead to drill smear if not properly addressed.

If drill smear is visible and bits are sharp, reduce chip load until it is eliminated.

Cutting Speed

Drill speeds of 100 SFM (30 m/min) are recommended. Slower speeds offer the greatest hole-quality improvements; they allow generated heat to dissipate before smearing PTFE. In certain stack ups, drill speed can be increased to 150-200 SFM (45-60 m/min) to improve productivity without sacrificing quality but added dwell times may become more important.

If drill smear is visible and bits are sharp, reduce cutting speed until it is eliminated.

Dwell Time

Lower surface speeds will reduce or eliminate the need for dwell. If ideal cutting speeds cannot be obtained, a 250ms dwell is recommended for initial process setup in order to cool the drill bit between holes and prevent softening of the PTFE that will later smear across interconnects. Past AGC studies have shown that hole-wall quality may improve as dwell times are increased to as much as 1000ms.

Peck Drilling

Peck drilling should be avoided where possible; it has been shown to increase drill bit wear as well as increase process time. Peck drilling may be required in some situations (e.g. bird nesting, hole plugging, chip extraction on thick panels, breaking thin drill bits, etc.). Peck drilling with a full withdrawal of the drill bit after each peck will reduce heat buildup and debris accrual. A general rule of thumb for peck depth is 20 to 30 mils per peck and should be optimized at the board shop.
If traditional peck drilling is not used, hole-wall quality may be improved with the use of a "clean" peck where the peck depth is set to equal that of the Phenolic entry. In this, the entry material will effectively clean the drill bit, retract to clear Phenolic debris and cool, and then reenter to drill the hole.

If tool breakage is an issue for small diameter, high aspect ratio holes, peck drilling may be inevitable. However, for 0.020" holes with an aspect ratio of roughly 12:1 or less, it is not clear that peck drilling is required. Some drill studies suggest that peck drilling will leave a small circular ring where the drill bits stop in the hole.

Hit Count

AGC recommends using new drills for the best hole quality. Hole wall quality will be directly related to drill bit hit count. To obtain high thermal conductivity while remaining economical to produce, RF-35TC and RF-60TC employ the use of a particularly abrasive ceramic filler. A conservative hit count with normal carbide bits is 50 hits/bit. 100-200 hits/bit can be used for less critical application. Less than hits/bit might be necessary if drill smear is a problem. Hit counts may improve in hybrid stack ups with only 1 or 2 thin cores of the TC material. Paying close attention to drill bit wear in these scenarios may provide longer drill life without sacrificing quality. Minimize hit counts as necessary to maintain hole wall quality. For very demanding hole wall specifications it might be necessary to drill the holes, pass the PCB through an electroless treatment or flash plating treatment to essentially make the debris in the hole rigid, then re-drill to snap the debris from the side of the hole wall. Another strategy for critical hole wall quality is to slightly under drill (using undersized diameter drill bit) the hole, thereby removing most of the PTFE-ceramic from the hole, flash plate the hole, and then re-drill it with the proper size bit. If undersized drilling is used, flash plating between drill sizes may not be necessary.

Entry / Backer Materials

Standard phenolic (0.024” thickness) and aluminum (0.007”-0.015”) entry material is recommended. Thicker phenolic (0.048” +) may be necessary on panels thicker than 0.200”. A phenolic backup board (from 0.040” to 0.125” thickness) such as LCOA Spectrum Gold is recommended to reduce bottom-side burring and drill smear. It is critical to fully plunge the drill bit into the phenolic backup to clean off debris before retracting the bit through the PCB and potentially re-depositing it on the hole wall. The addition of lubricated backups, such as Slickback, are optional but do provide some marginal effectiveness at reducing heat buildup on the drill bit, which ultimately leads to drill smear. Aluminum and phenolic serve to abrade Teflon debris off the bit. Optimizing the amount of phenolic to clean the drill tool between hits prevents bird nesting and smear and is a necessary factor in high quality RF-35TC and RF-60TC drilled holes. Do not worry about phenolic causing excessive drill wear. Although the process window is wider for drilling double sided PCBs vs. multilayer PCBs, one should follow the same strategies and tactics that one would use to fabricate a multilayer based on RF-35TC and RF-60TC cores. The pressure of the drill foot should be a minimum of 40 psi and should be increased if topside burring is excessive.

Laser Drilling / MicroVias

RF-35TC and RF-60TC Laminates

RF-35TC and RF-60TC are ideally laser drilled with a dual source laser (UV/CO2). It is possible to use a UV laser only at the potential expense of hole wall quality and reliability. Because of the high ceramic loading, most of the material removal is completed with the UV laser and the CO2 laser serves to remove any potential remaining PTFE from the microvia hole walls and the capture pad. The high ceramic loading also limits the anufacturability of microvias to a 0.005” thick laminate. Creating a microvia in a 0.010” thick laminate will require either a 2-step laser program (to dissipate heat), or a mechanical controlled depth drill (to remove the bulk of the material) followed by a laser drill to complete the microvia.

fastRise™

The lasing of the fastRise™ part numbers will vary between the different part numbers; please consult the fastRise™ datasheet for details regarding the ideal part numbers. Standard fastRise™ part numbers and those ending in “S” typically yield improved hole-wall quality. Shown below is a laser via through the FR-28-0040-50 part number.

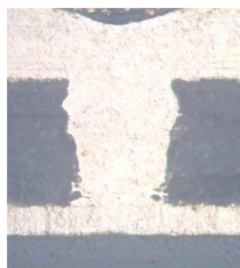


Photo by Hughes Circuits

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Hole Wall Preparation

RF-35TC and RF-60TC laminates require a PTFE activation cycle. If they are combined with fastRise™ in a multilayer PCB, the panels will benefit from a desmear/etchback process performed prior to the PTFE activation as directed below.

Desmear

Plasma

If panels have been exposed to moisture, bake the boards at 220°F - 250°F (105°C - 120°C) for 1 hour. Standard FR-4 desmear processes (CF_4/O_2) should then be used. The CF_4 desmear plasma time is typically half that of standard FR-4 times because the fastRise™ resin system tends to etch back very quickly.

Permanganate

A permanganate desmear IS NOT RECOMMENDED if the process contains glass etch chemistry. This is due to the high ceramic content of the fastRise™ resin system and will result in excessive etch back. Standard permanganate and glass etch baths as a part of the electroless copper process are OK. However, note that this alone will not sufficiently desmear the fastRise™ resin. A plasma process as described above is required for good hole wall quality.

PTFE Activation

Plasma

If panels have been exposed to moisture, pre-bake the boards at 220°F - 250°F (105°C - 120°C) for 1 hour. Plasma treat the PTFE resin using 70%/30% Hydrogen/Nitrogen gas mixture. 100% Helium may also suffice. Power settings for the RF-signal generator are typically 60-75% of full rated power for 30-60 minutes. Thick panels or high-aspect ratio holes may require extended plasma cycle times. Thick panels may also benefit from an additional 30 minute O_2 plasma process prior to the PTFE activation plasma. Experience has shown that gases such as Helium and CF_4 are not as effective as Hydrogen as evidenced by sporadic plating voids and higher contact angles. The advantage of plasma etching is that it is a relatively safe procedure. Disadvantages include relatively long cycle times (35 to 60 minutes) and short shelf life of the effect (4 – 24 hours).

Sodium Etch

Sodium Etches (e.g. Fluoroetch) work well with both fastRise™ and RF-35TC / RF-60TC laminates. Follow the manufacturer's recommended treatment process. Subsequently, bake for 1 hour at 250°F (120°C) prior to plating to remove moisture that may have been absorbed during the sodium treatment process.
The advantages of sodium etching include long shelf life of the hole wall treatment, fast treatment time, and complete coverage. The primary disadvantage of sodium etchant is the volatility of the chemical.

Chlorine can have adverse effects on the sodium treatment. Do not subject exposed sodium etch treated holes to heavily concentrated chlorine-based chemical processes.

Process Example

The following table is offered by March Plasma as a basic starting point recipe:

Power (kW)	Pressure (mT)	Gases	Gas Ratios	Flow (slm)	Pnl Temp (°C)	Time (minutes)	Function
4.5	250	O_2 / N_2	90 / 10	2.5	90	A/R	Heating
4	250	CF_4 / O_2	10 / 90	2.5	99	10	Thermoset etch-back
4	250	O_2	100	2.5	99	5	Removes fluorine and cleans the glass
4.2	250	H_2 / N_2	70 / 30	2.5	99	30	Activates PTFE. Alternative is 100% He gas

Note: Regardless of which method of hole wall treatment is used, desmearing of the thermoset resin should be done prior to treatment of the PTFE resin.

Plating

After the hole wall has been properly prepared, TSM-DS3 with fastRise™ will accept either electroless copper or direct metallization plating. The electrolytic plating process is the same for PTFE or epoxy based materials. Typical plating consists of 1 – 1.5 mils (25µm - 35µm) of copper plate in the holes and/or on the surface. For high-aspect ratios or other difficult to plate applications, a second pass through the electroless process may be required to ensure proper hole-wall coverage. It may also be beneficial to run a short duration of electrolyzed copper, rinse, etc., then restart the electrolyzed copper from the beginning to expose the hole wall to fresh chemistry.

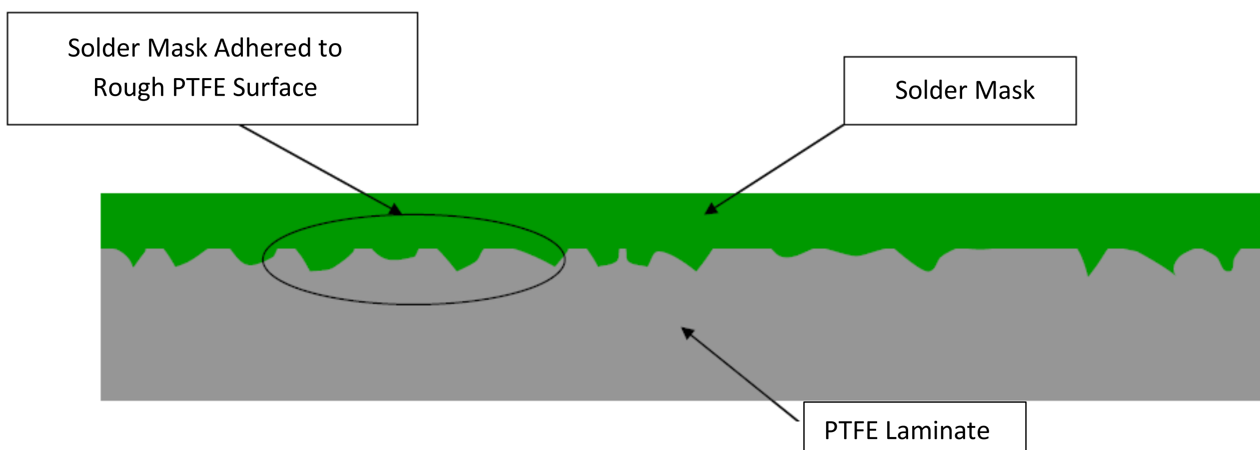
Image, Develop, Etch, Srtip

Prepare the copper surface, apply dry film, and image and develop using a standard process. The copper surface preparation should consist of microetching the copper. Mechanical scrubbing (e.g. pumice scrub) is not recommended for TSM-DS3 as the abrasion of the etched PTFE surface removes the left over surface topography required for good adhesion to photoresists. It may also cause distortion and registration issues if performed on inner layers or thin core subassemblies. The etching process is the same as for a standard printed circuit board. Machine settings should be appropriate for the copper thickness of the multilayer/inner layers. Strip the photoresist using a standard process.

SOLDER MASK

Overview

With the advantages of liquid photo imageable (LPI) soldermasks being their ease of use and resolution capability, they often do not have the same adhesion characteristics as the previous pure epoxy systems. This fact must be taken into account when applying LPI's to PTFE laminates. The mechanism for adhesion of soldermask (or prepreg or bonding film) to the PTFE laminate surface is the condition of the PTFE surface prior to application. By nature, PTFE is a very low surface energy fluoropolymer and thus it has excellent non-stick properties, which make it highly popular in lubrication and release applications. However, the adhesion of the base copper cladding is achieved by lamination of the relatively rough treated copper surface to the PTFE material under high heat and pressure. This process is able to produce an excellent mechanical bond between the PTFE resin and the rough dendritic surface of the copper. It is the negative impression of the rough copper treatment that remains in the PTFE after etching the copper to form the circuitry pattern, which provides adequate surface area for mechanical bonding of the soldermask to the PTFE surface. Therefore it is important to eliminate traditional scrubbing techniques which may disturb or destroy this rough surface.



With the need to replace the process a substitute process has been used which has several added benefits. Chemical cleaning of the copper surface offers the advantage of reduced mechanical stress on the material. This becomes critically important when dealing with thin laminates (<0.010" or 0.25 mm) and/or critical dimensional tolerances in soldermask or second stage drilling or routing. The removal of the scrubbing application also eliminates pits and dents which may be caused by high pressure contact with the steel or ceramic coated steel pinch rollers typically used in scrubbing machines to prevent panel movement during rotary scrubbing. In rare cases where adhesion is poor, a plasma treatment may be used to activate the exposed PTFE surface.

Pattern Plated Copper

1. Etch panels as normal to define circuitry pattern.
2. Allow plated metal etch resist (tin or tin/lead) to remain on panel through post etch inspectionprocesses to prevent copper surface contamination, staining or oxidation prior to soldermaskapplication.
3. Set up soldermask application process, prior to stripping or removing the metallic etch resist.
   Note: For double sided soldermask application, set up solder mask process to apply soldermaskto the side of the panel with the largest copper area to be covered (i.e. if the ground plane is tobe completely covered with soldermask then this would be the first side coated).
4. Strip tin or tin/lead from copper surfaces. The copper surfaces should be bright and stain freefollowing tin or tin/lead strip.
5. Chemically clean and roughen the copper surfaces using an acid or alkaline cleaner followed bya micro-etch process which removes 30-60 µin of copper. This should provide adequate surfacearea for adhesion of soldermask to copper surfaces.
6. Dry panels thoroughly. If you do not have an adequate horizontal dryer, then an oven bake isrecommended at 150-170°F [65-75°C] for 15-20 minutes.
   Note: Drying process should not causeoxidation of copper surfaces. If oxidation occurs, reduce drying time.
7. Allow panels to cool just enough so that they may be handled (approximately 5 minutes) andimmediately apply soldermask.
8. Tack dry (LPI) or bake and cure (silk screened epoxy) soldermask per manufacturer's recommendation.
9. Continue processing per manufacturer's recommendation for LPI soldermasks (image, develop and cure).
10. For second side, repeat processes beginning with # 5.

Panel Plated Copper

1. Etch panels as normal to define circuitry pattern.
2. Strip dry film resist from panels and rinse and dry thoroughly to prevent copper surface oxidation.
3. Using clean white cotton gloves, perform post etch inspection immediately following dry film removal. Move panels to soldermask process directly after inspection.
4. Set up soldermask application process while post etch inspection is taking place to minimize hold time between etch, strip and soldermask application.
   Note: For double sided soldermask applications, setup soldermask process to apply soldermask to the side of the panel with the largest copper area to be covered (i.e. if the ground plane is to be completely covered with soldermask then this would be the first side coated).
5. Chemically clean and roughen the copper surfaces using an acid or alkaline cleaner followed by a micro-etch process which removes 30-60 µin of copper. This should provide adequate surface area for adhesion of soldermask to copper surfaces.
6. Dry panels thoroughly. If you do not have an adequate horizontal dryer, an oven bake is recommended at 150-170°F (65-75°C) for 15-20 minutes.
   Note: Drying process should not cause oxidation of copper surfaces. If oxidation occurs, reduce drying time.
7. Allow panels to cool just enough so that they may be handled (approximately 5 minutes) and immediately apply soldermask.
8. Tack dry (LPI) or bake and cure (silk screened epoxy) soldermask per manufacturer's recommendation.
9. Continue processing per manufacturer's recommendation for LPI soldermasks (image, develop and cure).
10. For second side, repeat processes beginning with step # 5.

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Solder Reflow

When using hot air solder leveling on RF-35TC or RF-60TC, AGC recommends a bake cycle of 2 – 3 hours at 300°F (150°C) just prior to the HASL process. The solder pot temperature should be maintained at 460° – 480°F (240°C – 250°C) for optimal performance. Cycle time should be 5 – 6 seconds from the time of entry to the complete withdrawal of the board. Dwell time in the solder pot should not exceed 2 seconds. Longer preheat times and adjusted cycle times may be advantageous depending on design and processes.

Routing / Milling

Machining of RF-35TC and RF-60TC is typically more difficult than epoxy-based substrates due to the softness of the PTFE resin system combined with the abrasiveness of the ceramic filler. The low fiberglass content of these laminates does provide the advantage of reducing the amount of burring or exposed fibers left on the board edge. RF-35TC and RF-60TC can be successfully machined using two flute end mills when the recommended methods and rout parameters are used. Rigid phenolic entry and a rigid backer should be used. In some cases, adding paper (white paper or Kraft paper) between the phenolic and the part allows better conformance to surface topography (e.g. circuits, soldermask, etc.) and may reduce burring. For tight tolerances or superior edge quality, a “rough cut” placed 0.005 in. -0.010 in. off the part edge may be run prior to the “finish” cut at the nominal part edge. Historical data have yielded the following recommended rout parameters. These parameters are good starting points for PCBs comprised primarily of RF-35TC or RF-60TC. Special materials such as those with heavy metal ground planes may require different rout parameters and are not addressed in this guideline. More frequent bit changes are recommended. Router bit life should be established during initial setup of the routing process.

Router Diameter		Spindle Speed	Feed Rate	
(mils)	(mm)	(kRPM)	(in/min)	(m/min)
31.5	0.8	50	11.8	0.25
35.4	0.9	45	11.8	0.27
39.4	1.0	40	11.8	0.32
43.3	1.1	37	11.8	0.33
47.2	1.2	34	11.8	0.34
51.2	1.3	31	15.8	0.37
55.1	1.4	29	15.8	0.41
59.1	1.5	27	15.8	0.43
63.0	1.6	25	19.7	0.45
66.9	1.7	24	19.7	0.53
70.8	1.8	23	23.6	0.60
74.8	1.9	21	23.6	0.63
78.7	2.0	20	27.6	0.68
82.7	2.1	20	31.5	0.76
86.6	2.2	20	31.5	0.80
90.6	2.3	20	31.5	0.84
94.5	2.4	20	35.4	0.88
98.4	2.5	20	35.4	0.92
118.1	3.0	20	43.3	1.06
125	3.18	20	43.3	1.10

These guidelines can provide only basic and reference information for PCB fabricators. Because of different environment, equipment, tooling and so on, in all instances, the user shall determine suitability in any given conditions or applications. For more detailed processing information, please contact with the AGC engineer or sales representative.

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